

Remarks:

In the Office Action mailed on August 1, 2007, the Examiner rejected claims 1-31. Applicants amend claims 1, 4, 5, 7-9, 11, 12, 13, 19-22, 25, 28 and 30 herein. Applicants submit new claims 32 and 33. Claims 1-33 are pending in the application.

The Claims

Claim objections

Claims 19, 20 and 21 are objected to for the following informality: Claims were amended as follows “**wherein the write is carried out in an active physical area** if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, **the write is carried out in an active physical area.**” The Examiner indicated that he assumed Applicant meant to amend the claims such as amended claim 9 to state “where in if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area.” Applicants have amended Claims 19 – 21 to clarify the scope of the invention. Applicants posit that these amendments remove the informality and accordingly request withdrawal of the objection.

35 USC 112, second paragraph

Claims 1-31 were rejected under 35 USC 112, second paragraph as being indefinite for failing to comply with the written description requirement. Applicants have amended claims to more clearly recite the subject matter of the invention. Accordingly, Applicants respectfully request withdrawal of the rejection under 35 USC 112, second paragraph, and the allowance of Claims 1-31.

35 USC 103

Claims 1-2, 11, 13, and 23 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban (WO/94/20906) hereinafter Ban. Claims 3, 7-8, 18, 24, and 28-29 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1-2, 13, and 23 and in further view of Assar et al. (WO 95/10083) hereinafter Assar. Claims 4 and 25 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1 and 13 and further in view of Mennecart (WO 01/88926 A1) hereinafter Mennecart. Claims 5 and 26 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 2 and 13 and further in view of Hazen et al (WO 99/35650) hereinafter Hazen. Claims 6 and 27 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 26 and in view of Lipovski (US 5,758,148) hereinafter Lipovski. Claims 9-10 and 30-31 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1-2 and 13 and further in view of Kuo (US 4,763,305) hereinafter Kuo. Claim 12 is rejected under 35 U.S.C.103 (a) as unpatentable over Ban and further in view of Robinson et al (US 5,375,222). Claims 14-17 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 6 and further in view of Assar. Claims 19-20 and 22 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claim 5 and 6 and further in view of Kuo. Claim 21 is rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Assar as applied to claim 7 and further in view of Kuo.

While Ban, like applicant, addresses writing into a flash memory, Ban's approach is quite different from the method described and claimed by applicants.

In a flash type memory data is written by merely turning bits having the value zero to the value one. That, of course, only works if the bits that are to be zero after the write were already zero before the write.

Otherwise, the data location has to first be erased. Thus, writes normally involves zeroing out the data location and then writing the required one bits. Applicants address the issue that erasing a flash memory is a very costly operation in contrast to write operations. Thus, when an operation is performed that requires an erase operation, that operation is costly.

Applicant's solution is to associate a plurality of physical areas of the memory to each logical area. Then writes can be made by successively writing to these areas of memory that are each associated with the same logical area. Erase operations can be made when convenient, e.g., during idle moments. Thus, the write operations are generally optimized.

Applicants thus claim, "associating at least two physical areas of said memory, called mirror areas, with a same and unique logical area for storing a content" (Claim 1). One of the areas is "designat[ed] ... as being an active physical area", and "during a write to said logical area, programming the content of said logical are into the active physical area." (Claim 1).

Ban's solution does not teach or suggest these steps. While Ban organizes the memory into blocks and units, in writing to a unit, if a logical address is not free, an available free address is located. Ban, Page 9, lines 14-15. To reclaim memory, periodically all active blocks of one unit is copied into a unit, the TRANSFER unit, and the originating unit is flash erased. Ban, page 9, lines 23-26. However, there is no association of multiple physical areas of memory to a particular logical area as is claimed herein. Ban does not disclose or suggest a stationary association of a group of physical areas to a same and unique logical area.

Ban never discloses or suggests "associating at least two physical areas of the said memory ... with a same and unique logical area for storing a content." In Fig. 4, element 35, "a logical unit table 35 translates *the* logical unit number to *a* physical unit number for *the* logical unit" (Ban, page 8, lines 8-9) and "the logical address is mapped to *a* physical

address in the flash memory” (page 8, lines 22-23). Thus, it is clear that there is a one-to-one mapping in Ban between logical units and physical units. Nowhere does Ban say anything to the contrary.

The Examiner argues that something dynamic can be considered static because if something does not change even if considered dynamic then it was in fact static (“because a permanent is a special temporal case of dynamically capable”). Be that as it may. However, even so, there is no hint that there is a one-to-at least two mapping between logical and physical areas. Thus, even if the association table never changes, Ban has failed to teach or suggest Applicants’ claimed invention.

Thus, Claim 1 is not obvious over Ban and should be allowed.

Claims 11, 12, and 13 recite analogous limitations and should be allowed for, at least, the same reasons given in support of Claim 1.

Assar, Mennecart, Hazen, Lipovski, and Kuo are cited by the Examiner for propositions other than that argued hereinabove. None of those references teach or suggest “associating at least two physical areas of said memory, called mirror areas, with a same and unique logical area for storing a content; designating one of the physical areas as being an active physical area; and during a write to said logical area, programming the content of said logical area into the active physical area” (Claim 1 and analogous in the other independent claims). Therefore, Claim 1 and the other independent claims are patentable over these references taken singly, or in any combination including or not including Ban.

Therefore, because all the dependent claims depend from the independent claims, incorporate all the limitations thereof and provide further unique and non-obvious combinations, the dependent claims are patentable for, at least, the reasons given in support of the independent claims. (Applicants reserve the right to argue the independent

patentability of the various dependent claims in response to any further rejection of these claims)

The application is now deemed to be in condition for allowance and notice to that effect is solicited.

CONCLUSION

It is submitted that all of the claims now in the application are allowable. Applicants respectfully request consideration of the application and claims and its early allowance. If the Examiner believes that the prosecution of the application would be facilitated by a telephonic interview, Applicants invite the Examiner to contact the undersigned at the number given below.

Applicants respectfully request that a timely Notice of Allowance be issued in this application.

Respectfully submitted,

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